Listing of All Claims

1. (Currently amended) An apparatus comprising:

a first adder to add a first branch metric value to a previous path metric value to generate a first path metric value; and

saturating logic to detect a saturating condition when a most significant bit ("MSB") of said first path metric value is a specified value ~~and to responsively substitute~~;

the saturating logic arranged to select the first path metric value to form a first state metric when the saturating condition is not detected, and alternatively to select a predetermined maximum value to form the first state metric ~~for said first path metric value~~ when the saturating condition is detected.

2. (Currently amended) The apparatus as in claim 1 further comprising:

a comparator to compare said first ~~path~~ state metric ~~value or said predetermined maximum value with~~ to a second ~~path~~ state metric ~~value or said predetermined maximum value~~ transmitted from a second adder, and to responsively select a minimum one of said state metrics ~~values~~.

3. (Currently amended) The apparatus as in claim 2 further comprising:

an accumulator to store said selected minimum one of said first and second state metrics ~~values~~ for subsequent path metric calculations.

4. (Currently amended) The apparatus as in claim 1 wherein said saturating logic comprises:

a multiplexer to select between said predetermined maximum value and said ~~new~~ first path metric value, wherein said value of said MSB operates as selection logic to control said multiplexer.

5. (Currently amended) The apparatus as in claim 3 wherein said predetermined maximum value is a maximum value that ~~may~~ can be stored by said accumulator.

6. (Original) The apparatus as in claim 1 wherein said predetermined maximum value is 7h7f.

7. (Currently amended) The apparatus as in claim 2 further comprising:

a plurality of additional comparators to compare ~~path~~ state metric values and select a minimum for a plurality of additional accumulators.

8. (Original) The apparatus as in claim 7 wherein the total number of accumulators is equal to a Viterbi trellis depth.

9. (Original) The apparatus as in claim 7 wherein the total number of accumulators is equal to 64.

10. (Currently amended) A ~~computer-implemented~~ decoding method comprising:

adding a first branch metric value to a previous path metric value to generate a first path metric value; ~~and~~

detecting a saturating condition when a most significant bit ("MSB") of said first path metric value is a specified value; and

~~responsively substituting a predetermined maximum value for said first path metric value.~~

selecting the first path metric value as a first state metric when the saturating condition is not detected, and alternatively selecting a predetermined maximum value as the first state metric when the saturating condition is detected.

11. (Currently amended) The method as in claim 10 further comprising:

comparing said ~~first path metric value or said predetermined maximum value~~ first state metric with a second ~~path~~ state metric ~~value or said predetermined maximum value~~ transmitted from a second adder; and

~~responsively~~ selecting a minimum one of said ~~values~~ state metrics.

12. (Currently amended) The method as in claim 11 further comprising:

storing said selected minimum one of said ~~values~~ state metrics for subsequent path metric calculations.

13. (Currently amended) The method as in claim 10 wherein ~~substituting~~ selecting comprises:

configuring a multiplexer to select between said predetermined maximum value and said ~~new~~ first path metric value, wherein said value of said MSB operates as selection logic to control said multiplexer.

14. (Currently amended) The method as in claim 12 wherein said predetermined maximum value is a maximum value that ~~may~~ can be stored by said accumulator.

15. (Original) The method as in claim 10 wherein said predetermined maximum value is 7h7f.

16. (Currently amended) The method as in claim 12 further comprising:

comparing ~~path~~ state metric values and selecting a minimum for a plurality of additional accumulators.

17. (Original) The method as in claim 16 wherein the total number of accumulators is equal to a Viterbi trellis depth.

18. (Original) The method as in claim 10 wherein the total number of accumulators is equal to 64.

19. (Currently amended) ~~A machine-readable medium having code stored thereon which defines an~~ An integrated circuit (IC), ~~said IC~~ comprising:

a first adder to add a first branch metric value to a previous path metric value to generate a first path metric value; and

saturating logic to detect a saturating condition when a most significant bit ("MSB") of said first path metric value is a specified value ~~and to responsively substitute;~~

the saturating logic arranged to select the first path metric value to form a first state metric when the saturating condition is not detected, and alternatively to select a predetermined maximum value to form the first state metric ~~for said first path metric value~~ when the saturating condition is detected.

20. (Currently amended) The ~~machine-readable medium~~ integrated circuit as in claim 19 further comprising:

a comparator to compare said first ~~path~~ state metric ~~value or said predetermined maximum value with~~ to a second ~~path~~ state metric ~~value or said predetermined maximum value~~ transmitted from a second adder, and to responsively select a minimum one of said state metrics ~~values~~.

21. (Currently amended) The ~~machine-readable medium~~ integrated circuit as in claim 20 wherein said IC further comprises:

an accumulator to store said selected minimum one of said ~~values~~ first and second state metrics for subsequent path metric calculations.

22. (Currently amended) The ~~machine-readable medium~~ integrated circuit as in claim 19 wherein said saturating logic comprises:

a multiplexer to select between said predetermined maximum value and said ~~new~~ first path metric value, wherein said value of said MSB operates as selection logic to control said multiplexer.

23. (Currently amended) The ~~machine-readable medium~~ integrated circuit as in claim 21 wherein said predetermined maximum value is a maximum value that ~~may~~ can be stored by said accumulator.

24. (Currently amended) The ~~machine-readable medium~~ integrated circuit as in claim 19 wherein said predetermined maximum value is 7h7f.

25. (Currently amended) The ~~machine-readable medium~~ integrated circuit as in claim 20 ~~wherein said IC~~ further comprising:

a plurality of additional comparators to compare ~~path~~ state metric values and select a minimum for a plurality of additional accumulators.

26. (Currently amended) The ~~machine-readable medium~~ integrated circuit as in claim 25 wherein the total number of accumulators is equal to a Viterbi trellis depth.

27. (Currently amended) The ~~machine-readable medium~~ integrated circuit as in claim 25 wherein the total number of accumulators is equal to 64.

28. (New) A method for use in a digital decoder comprising the steps of:

determining a branch metric distance value;

monitoring a path metric accumulator value;

responsive to the path metric accumulator value reaching a first predetermined value, normalizing the path metric accumulator value by:

selecting a normalization quantity;

adding the selected normalization quantity to the branch metric distance value to form a sum; and

inputting the sum to the path metric accumulator, thereby adding the selected normalization quantity to the path metric accumulator value to normalize it.

29. (New) A method according to claim 28 wherein:

said monitoring is conducted over multiple path metric accumulator values; and

said normalizing step is triggered only when all of the monitored path metric accumulator values exceed the first predetermined value.

30. (New) A method according to claim 29 wherein selecting the normalization quantity includes selecting one among a plurality of predetermined normalization quantities.

31. (New) A method for use in a digital decoder comprising the steps of:

monitoring bit settings in each of a plurality of path metric accumulators, each accumulator providing a respective path metric accumulator value during a decoding operation;

detecting when all of the path metric accumulator values reaches at least a first predetermined value; and

responsive to all of the path metric accumulator values reaching at least the first predetermined value, selecting a normalization value and adding the selected normalization value to each of the path metric accumulators to normalize the accumulators.

32. (New) A method according to claim 31 wherein the normalization value is selected from at least two predetermined normalization values.

33. (New) A method according to claim 31 wherein said adding the selected normalization value comprises adding the selected normalization value to a branch metric

value, and then updating the path metric accumulator with a sum of the branch metric value plus the selected normalization value.

34. (New) A method according to claim 33 wherein selecting the normalization value includes selecting a negative normalization value so as to reduce the path metric accumulator value.

35. (New) A method according to claim 31 wherein selecting the normalization value is based on the current bit settings of at least two MSB's of the accumulator value.

36. (New) A method according to claim 31 wherein selecting the normalization value includes selecting a negative normalization value having a magnitude equal to 2^N where N is a bit position of a most significant bit of the accumulator that is set.

37. (New) An add-compare-select (ACS) circuit for use in a digital decoder apparatus comprising:

a first adder for adding a first branch metric value to a first path metric value to form a first sum;

saturation logic for detecting a saturation condition in the first adder; and

a first multiplexer responsive to the saturation detecting logic for selecting either the first sum or a predetermined saturation value as a first state metric output.

38. (New) An add-compare-select (ACS) circuit according to claim 37 and further comprising:

second adder for adding a second branch metric value to a second path metric value to form a second sum;

second saturation logic for detecting a saturation condition in the second adder;

a second multiplexer responsive to the second saturation detecting logic for selecting either the second sum or a predetermined saturation value as a second state metric output; and

a comparator for comparing the first and second state metric outputs.

39. (New) An add-compare-select (ACS) circuit according to claim 38 wherein the saturation value is selected as a maximum output value of the first adder.